REMARKS

Claims 1-23 remain active in the Application.

Claims 1-12, 14-17, and 19-23 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Patra, Pryadarsan et al. (U.S.P. 6,529,861 B1) (Patra) in view of Chakradhar et al. (S.T. Chakrahdar, A. Balakrishnan, and V. D. Agrawal, "An exact algorithm for selecting partial scan flip-flops", 1994 Design Automation Conference, pages, 81-86) (Chakradhar).

Applicants respectfully traverse the above started rejection for the following considerations:

Applicants have reviewed the subject Office Action, and do not believe that the prior art cited by the Examiner in any way makes renders the above cited claims unpatentable under 35 U.S.C. 103(a) over Patra a in view of Chakradhar. These references address totally different problems, and their solutions do not apply to the problem addressed by the present invention.

Applicants submit that independent claims 1, 22, and 23 specifically include building a scan chain based on result values probabilities such that it reduces switching activity **as determined by ordering the memory elements within the scan chain**. Neither of the prior art references, whether taken independently or in combination, even mentions the ordering of memory elements in a scan chain, let alone teaching any manner in which such an ordering can affect switching activity during scanning.

Chakradhar et al. teach a method of determining which memory elements should be included in scan chains, by determining an MFVS (Minimum Feedback Vertex Set) of an S-graph representing the functional logic connections (not scan connections) between memory elements. However, once this set has been determined, there is no mention about how these memory elements should be connected into scan chains.

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Patra teaches a method of reducing the switching activity and hence power of domino logic, but their method is exclusively limited to domino logic. In fact, in col. 5, lines 22 - 23, it states that "The phase assignment only affects power consumption if the circuit is implemented in domino logic." It further states on lines 31-33 that "...the symmetric behavior of CMOS gates prevents the phase assignment from affecting the switching activity." Thus, the method taught by Patra is specific to a particular type of combinational logic (which is what domino logic is used to implement) and does not address power consumption due to ordering of memory elements in scan chains.

Although Chakradhar et al. discusses scan chains, no mention is made regarding the ordering or phase assignment within them. Furthermore, Patra discusses phase assignment at inputs and outputs of combinational logic, but specifically does so in such a way that the phase of the memory elements feeding and fed by the combinational logic is preserved (by optionally inserting inverters at the inputs ad outputs of combinational logic sections). Thus, the respective methods are restricted to making changes which do not alter the net inversion along a functional logic path between a source and sink memory element. The phase assignment in the present invention, however, relates to the connections between elements in a scan chain. In this case the choice of which connections are to be made (i.e., which memory elements are to be placed adjacent to one another in the scan chain) and whether or not such the connections should be inverted, a degree of freedom specifically not taught by Chakradhar

Thus, the present invention teaches away from the teachings of Patra and Chakradhar, whether taken individually or in combination. Further, the present invention, as recited in Claims 1, 22 and 23 addresses a different problem than that the cited art references, and the claims of the present invention include specific reference to ordering of scan chains to reduce switching activity, which neither of these references discusses altogether.

Claims 2-13 and 18 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Patra, Pryadarsan et al. (U.S.P. 6,529,861 B1) (Patra) in view of Chakradhar et al.

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Claims 2-13 and 18 are dependent on claim 1. Accordingly, the previous arguments regarding the ordering of memory elements in scan chains which is lacking in both Patra and Chankradhar also apply to the claims dependent on claim 1.

Claims 14-17 and 19-21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Patra in view of Kajihara. (On Identifying Don't Care Inputs of Test Patterns for Combinatorial Circuits (ICCAD 2001, pages 364-369) (Kajihara).

Claims 14-17 and 19-21 also depend on claim 1. As previously stated, Patra does not address the ordering of memory elements in scan chains. Neither does Kajihara. Thus, the combination of Patra and Kajihara does not render claim 14-17 and 19 unpatentable over Patra in view of Kajihara.

Thus, Applicants believe that the rejection of claims 1-23 under 35 U.S.C. 103(a) as being unpatentable over Patra in view of Chakradhar et al. has been overcome, and respectfully request that the Examiner reconsider and withdraw the rejection of the stated claims based thereon.

In view of the foregoing arguments, Applicants respectfully request that all the rejections and objections to this application be reconsidered and withdrawn and that the Examiner pass all the pending claims to issue.

Should the Examiner have any suggestions pertaining to the allowance of the application, the Examiner is encouraged to contact Applicants' undersigned representative.

Respectfully submitted,
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